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09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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EXAMINER

NGUYEN, KEVIN M

ART UNIT PAPER NUMBER

2674

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/211,677

Applicant(s)

LEE, HYUN CHANG

Examiner

Kevin M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 27-37 and 56-88 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27-37 is/are allowed.
- 6) ☒ Claim(s) 56-88 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11/15/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. This office action is made in response to applicant's amendment filed on 11/15/2004. Claims 1-26, 38-55 are cancelled, claim 82 is amended, and claims 27-37, 56-88 are currently pending in the application. An action follows below:

Drawings

2. The objection of drawing 13 is withdrawn. The drawings were received on 11/15/2004. These drawing 11A and 11B are acknowledged.

Response to Arguments

3. Applicant's argument, see page 12, filed 11/15/2004, with respect to claims 27-37 have been fully considered and are persuasive. The rejection of claims 27-37 has been withdrawn.

Allowable Subject Matter

4. Claims 27-37 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

Based on applicant's argument at page 12, none of cited prior arts fails to teach or suggest "wherein the second voltage is near the data signal voltage..."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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6. Claims 56-88 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al (US 5,587,722).

As to claims 56, 62, Suzuki et al teaches an active matrix liquid crystal display device associated with a method, the apparatus comprising:

[recited in lines 2-7 of claim 56]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

a clock driver (a scanning clock signal as claimed) for supplying clock pulses Vck1 and Vck2 and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

[recited in lines 8-13 of claim 56]

According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called 1H-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30).

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As described above, it is possible to suppress the voltage shift of the video signals by shaping a fall of the gate pulses smoothly or step-wisely (col. 6, lines 31-33).

As to claims 71 and 76, Suzuki et al teaches an active matrix liquid crystal display device associated with a method, the apparatus comprising:

[recited in lines 2-12 of claim 71]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

a clock driver (a timing controller as claimed) for supplying clock pulses Vck1 and Vck2 and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

[recited in lines 13-22 of claim 71]

According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called 1H-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30).

As described above, it is possible to suppress the voltage shift of the video signals by shaping a fall of the gate pulses smoothly or step-wisely (col. 6, lines 31-33).

As to claims 28-32, 57-61, 63, 77-80, Suzuki et al teaches in the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals V_{sig} is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level V_{gate1} of the gate pulses GP to be the value of V_{gate2} directly before a transition from the selected period of time to the non-selected period of time (col. 3, lines 52-57).

the n -th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP ($n+1$) corresponding to the ($n+1$)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely (col. 6, lines 16-21).

As to claims 33, Suzuki et al teaches a clock driver (a timing controller as claimed) for supplying clock pulses V_{ck1} and V_{ck2} and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

As to claims 36, Suzuki et al teaches wherein gate pulses GP are applied to a gate electrode of each transistor during a selected period of time for writing video signals V_{sig} to each pixel, and the applying of the gate pulses GP is stopped in a non-selected period of time for holding the written video signals V_{sig} , thereby performing the video display (col. 3, lines 20-25).

As to claims 37, 67, Suzuki et al teaches a central point between a pair of potential dividing resistance $R1$ and $R2$ (a second voltage source as claimed, col. 5,

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lines 34-35) and the other end is connected to the side of the ground (col. 5, lines 36-38).

As to claims 34, 64, Suzuki et al teaches a vertical scanning circuit 1, a gate driver comprising a shift register 3 (fig. 2, col. 5, lines 49-50).

As to claims 65, 68-70, 72-75, 81, Suzuki et al teaches

Recited at col. 5, lines 39-47,

A gate electrode of the switching transistor 14 is periodically applied with a control voltage VCKX. When the switching transistor 14 is in the off-state, the supply voltage is supplied to a shift register 3 as it is, and the voltage level of each gate pulse GP is equal to the supply voltage. On the other hand, when the switching transistor 14 is in the on-state, the voltage divided with the ratio $R1/R2$ is supplied to the shift register 3, and thereby the voltage level of the gate pulse GP is reduced

Recited at col. 6, lines 10-15,

As the control voltage VCKX becomes the high level, the switching transistor 14 is in the on-state, so that the level of the supply voltage supplied to the shift register 3 is reduced, for example, from the VVDD set at 13.5 V (a first voltage as claimed) to the about 8.5 V (a second voltage as claimed).

Recited at col. 3, lines 52-57,

In the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals Vsig is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level Vgate1 of the gate pulses GP to be the

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value of V_{gate2} directly before a transition from the selected period of time to the non-selected period of time.

As to claim 82, Suzuki et al teaches an active matrix liquid crystal display device comprising:

[recited in lines 2-9 and 14-15 of claim 82]

Referring to fig. 3, a pixel LP, a switching transistor T_r , a video signal V_{sig} , a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

[recited in lines 8-13 of claim 82]

In the potential dividing resistances $R1$ and $R2$, one end is connected to the power supply V_{VDD} (a first voltage source as claimed) and the other end is connected to the side of the ground through a switching transistor 14 (col. 5, lines 36-41).

a central point between a pair of potential dividing resistance $R1$ and $R2$ (a second voltage source as claimed, col. 5, lines 34-35)

As the control voltage V_{CKX} becomes the high level, the switching transistor 14 is in the on-state, so that the level of the supply voltage supplied to the shift register 3 is reduced, for example, from the V_{VDD} set at 13.5 V (a first voltage as claimed) to the about 8.5 V (a second voltage as claimed) (col. 6, lines 10-15).

As to claims 83, 84, Suzuki et al teaches in the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals V_{sig} is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level V_{gate1} of the gate pulses GP to be the value of V_{gate2} directly before a transition from the selected period of time to the non-selected period of time (col. 3, lines 52-57).

the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely (col. 6, lines 16-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 35, 85, 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al in view of Applicant's Admitted Prior Art hereinafter AAPA.

As to claims 35, 85, 86, Suzuki et al teaches all of the claimed limitations, except for the gate signal line includes a distributed series resistance and a distributed capacitance.

However, AAPA discloses the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 (see figure 3, page 5, lines 2-5). Since a waveform modifying circuit such as an integrator for each gate line must be added (page 5, lines 30-32).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Suzuki's gate signal line including a distributed series resistance R1 and a distributed capacitance C1, in view of the disclosing AAPA

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because this would eliminate flickering and residual image (see page 5, lines 29-30 of AAPA).

Response to Arguments

8. Applicant's arguments filed 11/15/2004 have been fully considered but they are not persuasive.

9. In response to applicant's argument that claims 56, 62 recite "said first voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor," This argument is not persuasive because Suzuki et al teach, as mentioned above, "According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called 1H-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30). As described above, it is possible to suppress the voltage shift of the video signals by shaping a fall of the gate pulses smoothly or step-wisely (col. 6, lines 31-33).

Thus, the teaching of Suzuki's reference provides and establishes the "substantial evidence" to produce and result the claimed limitations of claim 56, for example, shaping a fall of the gate pulses smoothly defined inherently the claimed limitation "substantially to a threshold voltage level."

During this period of time, in the video signals Vsig,... the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses defined the claimed limitation "but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage."

the potential Vcom defined the claimed limitation "wherein the second gate voltage has a voltage level that turns off the switching transistor."

10. In response to applicant's argument that claim 71 recites "said first voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching device during the period of the scanning clock signal prior to the driver selecting the successive scanning line." This argument is not persuasive because Suzuki teaches shaping a fall of the gate pulses smoothly defined inherently the claimed limitation "substantially to a threshold voltage level." During this period of time, in the video signals Vsig,... the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses. Fig. 4 shows expressly "a horizontal period" which defined the scanning clock signal period prior to the driver selecting the successive scanning line as claimed.

11. In response to applicant's argument that claim 76 recites "said first voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain

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a connection between the plurality of contact electrodes to the plurality of pixel electrodes prior to applying the second gate voltage.” This argument is not persuasive because Suzuki teaches shaping a fall of the gate pulses smoothly defined inherently the claimed limitation “substantially to a threshold voltage level.” During this period of time, in the video signals Vsig,... the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses. Fig. 4 shows expressly “the waveform GP (n+1) is after the waveform GP (n)” and “waveform Vsig is ON at negative pulse at period of the waveform GP (n), and is ON at the positive pulse the waveform GP (n+1), which defined a connection between the plurality of contact electrodes to the plurality of pixel electrodes prior to applying the second gate voltage as claimed.

12. In response to applicant's argument that claim 82 recites “the high level gate voltage generator including a means for modulating the first voltage level of the gate voltage.” This argument is not persuasive because a person of ordinary skill in the art to understand that Fig. 4 shows expressly the waveform GP (n) at the horizontal period which has the pulse was modulated/adjust the voltage values from 13.5V to 8.5V during 6-8μsec. Thus, the teaching of Suzuki's fig. 4 provides and establishes the “substantial evidence” to produce and result the claimed limitations of claim 82.

For these reasons, the rejections based on Suzuki et al have been maintained.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

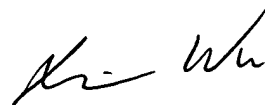
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(toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KMN
April 29, 2005



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PRIMARY EXAMINER